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Implementation if Low Power SOC Zigbee Baseband Processor Processor with I2C Interface

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Abstract *:* The rapid growth experienced by the wireless communication sector in recent years is conspicuous. There are many wireless monitoring and control applications for industrial and home markets which require longer battery life, lower data rates and less complexity than available from existing wireless standardsThe ZigBee protocol is adopted for wireless communication to achieve high integration, applicability, and portability. The low-power Zigbee-SoC is simulated by the altera modelsim 6.4a. Here proposed Zigbee transceiver with i2c to implement wireless communication applications.
Keywords *:* *Altera , OQPSK, Symbol to Chip*

I. INTRODUCTION

ZigBee is a wireless networking standard that is aimed at remote control and sensor applications which is suitable for operation in harsh radio environments and in isolated locations. ZigBee technology builds on IEEE standard 802.15.4 which defines the physical and MAC layers. Above this, ZigBee defines the application and security layer specifications enabling interoperability between products from different manufacturers. In this way ZigBee is a superset of the 802.15.4 specification. With the applications for remote wireless sensing and control growing rapidly it is estimated that the market size could reach hundreds of millions of dollars as early as 2007. This makes ZigBee technology a very attractive proposition for many applications.

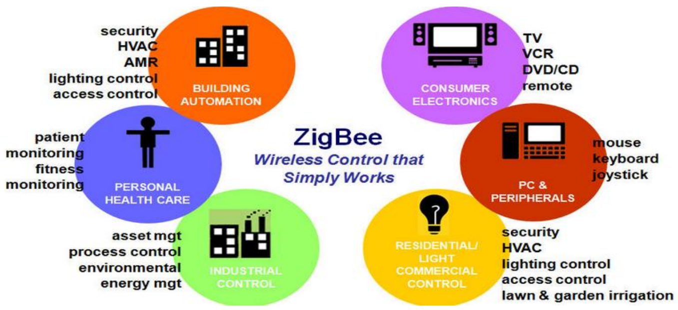

Fig 1 : Areas of Zigbee

ZigBee is a wireless technology developed as an open global standard to address the unique needs of low-cost, low-power, wireless sensor networks. The standard takes full advantage of the IEEE 802.15.4 physical radio specification and operates in unlicensed bands worldwide at the following frequencies: 2.400–2.484 GHz, 902-928 MHz and 868.0–868.6 MHz. Where the 2.45 GHz ZigBee possesses 16 channels which has the highest transmission bit rate owing to that the O-QPSK (offset-quadrature phase shift keying) modulation is employed. The expected bit rate is 250Kbps (62.5 KSymbols/s) which are sufficient for conveying security information or personal medical monitoring usage

II. EXISTING SYSTEM

The distances that can be achieved transmitting from one station to the next extend up to about 70 metres, although very much greater distances may be reached by relaying data from one node to the next in a network. The main applications for 802.15.4 are aimed at control and monitoring applications where relatively low levels of data throughput are needed, and with the possibility of remote, battery powered sensors, low power consumption is a key requirement. Sensors, lighting controls, security and many more applications are all candidates for the new technology.

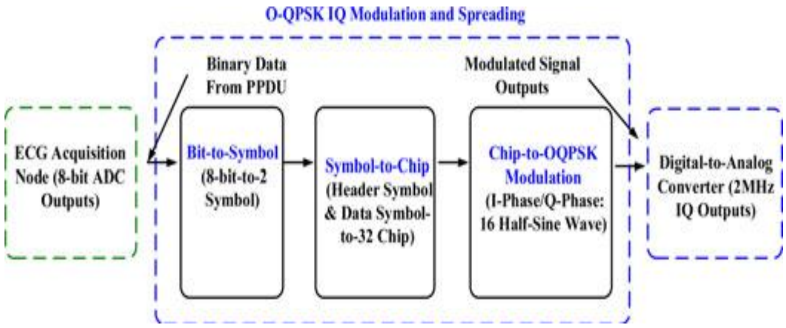

Fig 2: Zigbee Transmitter

III. Proposed Zigbee Transceiver

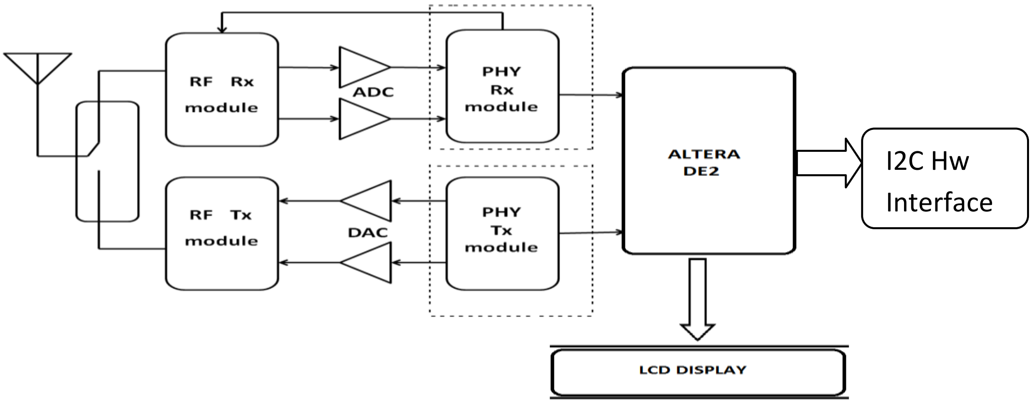

Fig 3 : Proposed Low Power Zigbee Transceiver Functional Diagram

The above block diagram of the proposed ZigBee transceiver with I2C sensor interface module make hardware architecture to achieve low power control applications, at very high faster date rates. The RF signal is down-converted to baseband by the RF receiver (Rx) and quantized by the analog -to-digital converters (ADC). These digital signals are sent to the LCD display. It displays transmitted data after the digital demodulation performed by the proposed Rx. The original analog data is reconverted by digital to analog converter. Then it is transmitted by RF transmitter(Tx).In addition to that low power I2C sensor interface module is interconnected for serialised control appliances.

IV. TRANSMITTER BLOCK

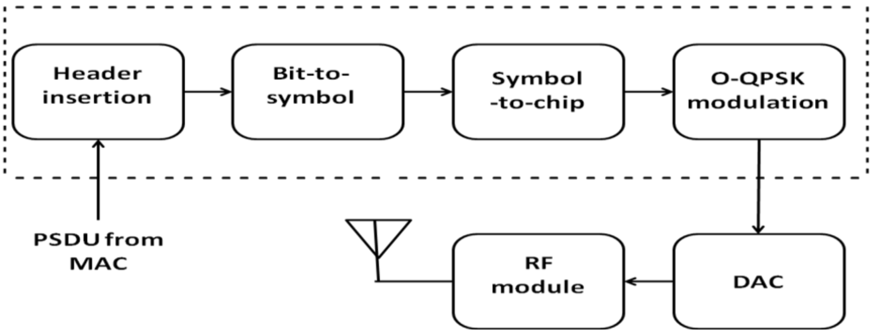

Fig 4 : Transmitter block diagram

The proposed ZigBee Tx is based on IEEE standard wireless Personal Area Network. From the serial inputs, every 4 bits are mapped into one data symbol. The symbol-to-chip stage performs the direct-sequence spread spectrum (DSSS), where each symbol is mapped into a 32-chip pseudo-random noise (PN) sequence. Notably, the O-QPSK modulation is adopted in 2.45 GHz mode. The fundamental O-QPSK method is to sum the in-phase signal with quadrature phase signal delayed by half a cycle in order to avoid the sudden phase shift change. Then, the modulated O-QPSK signal goes along with the pulse shaping stage to reduce the inter-symbol interference (ISI). Each baseband chip is represented as a half-sine pulse shape. The resultant signal is transmitted by the RF transmitter.

Table 1 symbol to chip

Decimal value	Binary value	Chip value
00	0000	11011001110000110101001000101110
01	0001	11101101100111000011010100100010
02	0010	00101110110110011100001101010010
03	0011	00100010111011011001110000110101
04	0100	01010010001011101101100111000001
05	0101	00110101001000101110110110011100
06	0110	11000011010100100010111011011100
07	0111	10011100001101010010001011101101
08	1000	10001100100101100000011101111011
09	1001	10111000110010010110000001110111
10	1010	01111011100011001001011000000111
11	1011	01110111101110001100100101100000
12	1100	00000111011110111000110010010110
13	1101	01100000011101111011100011001001
14	1110	10010110000001110111101110001100
15	1111	11001001011000000111011110111000

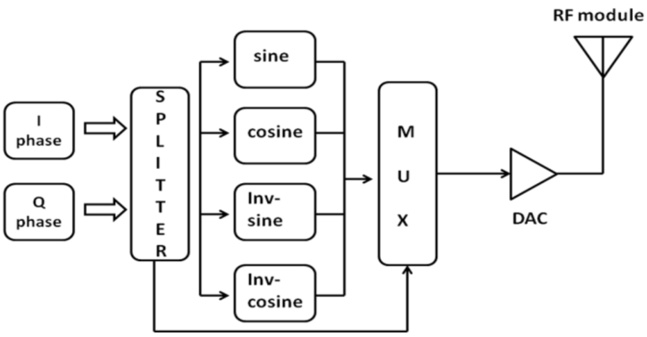

Fig 5: O-QPSK Modulator Block Diagram

The spread signal is modulated O—QPSK modulation divides the input data (chips) by a multiplexer generating two channels called pair sequence or in phase (I) and odd sequence or quadrature phase (Q). The Q channel adds a delay of half a chip period. Then I and Q data are given to the splitter unit.

V. Receiver Block

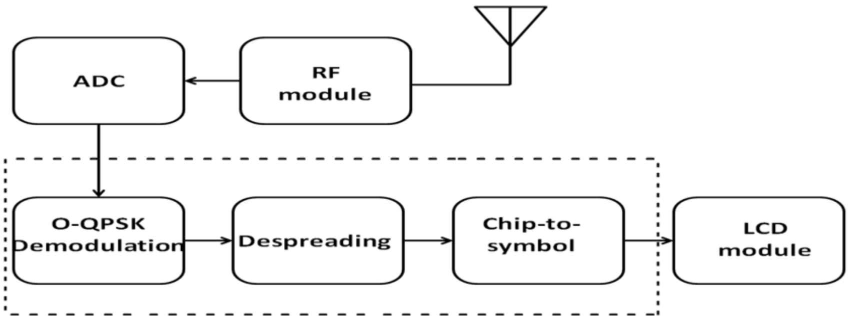

Fig 6: Receiver Block Diagram

In the block diagram of the ZigBee Rx, once the data starts receiving it enables other stages. Each 32-chip PN sequence is sampled to be 128 samples by the ADC. The Demodulator stage utilizes the minimum shift keying (MSK) scheme to perform the demodulation process. The reason is that MSK is a special case of O-QPSK with sinusoidal symbol weighting, which can be no coherently detected. Hence, the proposed Rx adopts the MSK demodulation to implement a receiver which possesses lower hardware complexity. The despreading stage despreads each 32-chip PN sequence to 4-bit symbols. The output from the despreader block is given to the LCD module for display the data.

VI. SIMULATION RESULTS

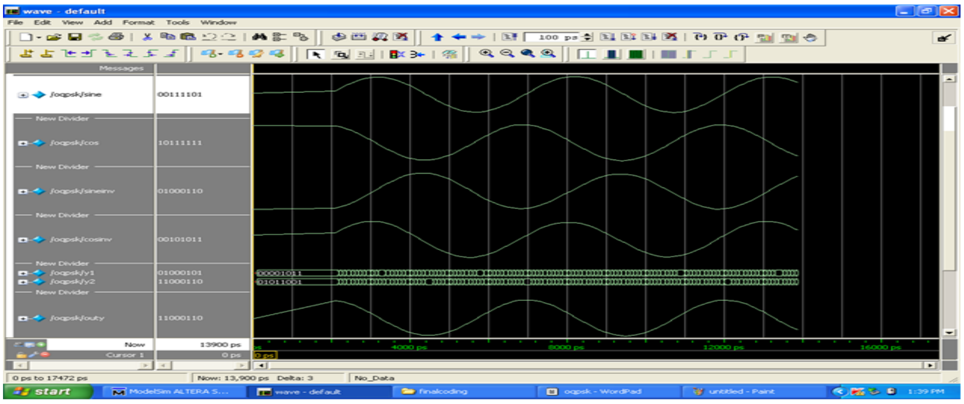

Fig 7: O-QPSK Modulator simulation output

O-QPSK scheme used by most high speed modems, allows quicker data transfer than FSK. And it gives at least four states to send information. Offset Quadrature phase shift keying changes a sine wave's normal pattern. It shifts or alters a wave's natural fall to rest or 0 degrees. By forcing changes in a sine wave we can convey information. As an example, 90 degrees, 0 degrees, 180 degrees, and 270 degrees might be represented by binary digits 00, 01, 10, and 11 respectively

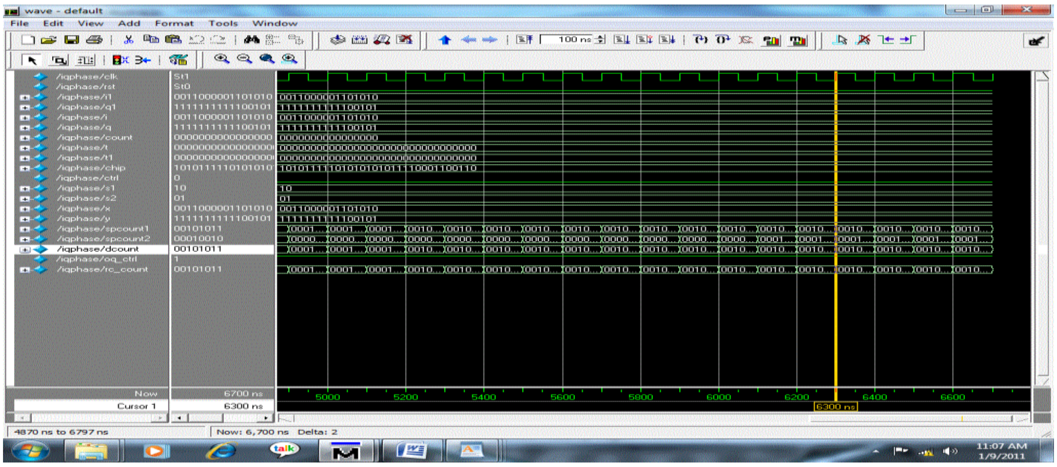

Fig 8: Zigbee with i2c output

The spread signal is modulated O—QPSK modulation divides the input data (chips) by a multiplexer generating two channels called pair sequence or in phase (I) and odd sequence or quadrature phase (Q). The Q channel adds a delay of half a chip period. Then I and Q data are given to the splitter unit

VII. CONCLUSION

The module for "implementation of Zigbee transceiver using FPGA" has been designed as per the block diagram. During the implementation stage, the operation of Zigbee transceiver as tested using Altera Mentor Graphics Modelsim 6.4a. The simulation result shows how the data gets modulated in transmitter section and the demodulation in the receiver section.

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